NMUX27518

6-channel, 1-of-2 multiplexer and demultiplexer

Rev. 1 — 25 July 2025 | Product data sheet

1. General description

The NMUX27518 is a bidirectional, 6-channel, 1:2 multiplexer-demultiplexer designed to operate from 1.08 V to 3.6 V. This device can handle both digital and analog signals, and can transmit signals up to V_{CC} in either direction. The NMUX27518 has two control pins (S0, S1), each controlling three 1:2 muxes at the same time, and an enable pin ($\overline{EN}$) that put all outputs in high-impedance mode. The control pins are compatible with 1.8 V logic thresholds and are backward compatible with 2.5 V and 3.3 V logic thresholds.

2. Features and benefits

- Wide operating range: 1.08 V to 3.6 V
- Isolation in power-down mode, V_{CC} = 0 V
- Low-capacitance switches, 21.5 pF (typical)
- Bandwidth up to 500 MHz for high-speed rail-to-rail signal handling
- Crosstalk and isolation OFF-state: –62 dB
- 1.8 V logic compatible control inputs
- 3.6 V tolerant control inputs
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2 kV
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1.5 k V
  - IEC61000-4-2, level 3, contact discharge on all nYn pins exceeds ±6 kV
- 24 pins TSSOP24 (7.8 x 4.4 x 1.1 mm body) and HWQFN24 (4 × 4 × 0.75 mm body) packages
- Specified from -40 °C to +125 °C

3. Applications

- SD-SDIO and MMC two-port MUX
- PC VGA video MUX-video systems
- Audio and video signal routing

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4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NMUX27518PW	-40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
NMUX27518BY	-40 °C to +125 °C	HWQFN24	plastic thermal enhanced very very thin Quad Flat packages; no leads; 24 terminals; 0.5 mm pitch; 4 × 4 × 0.75 mm body	SOT8041-1

5. Marking

Table 2. Marking

Type number	Marking code
NMUX27518PW	NMUX27518
NMUX27518BY	M27518

6. Functional diagram

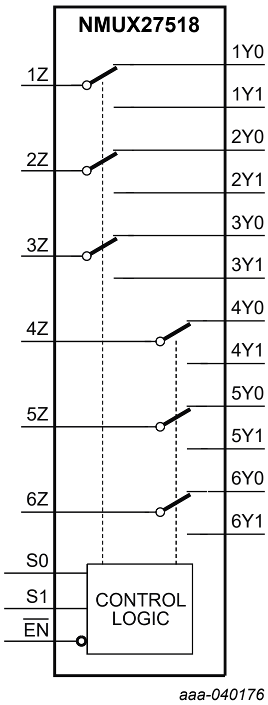
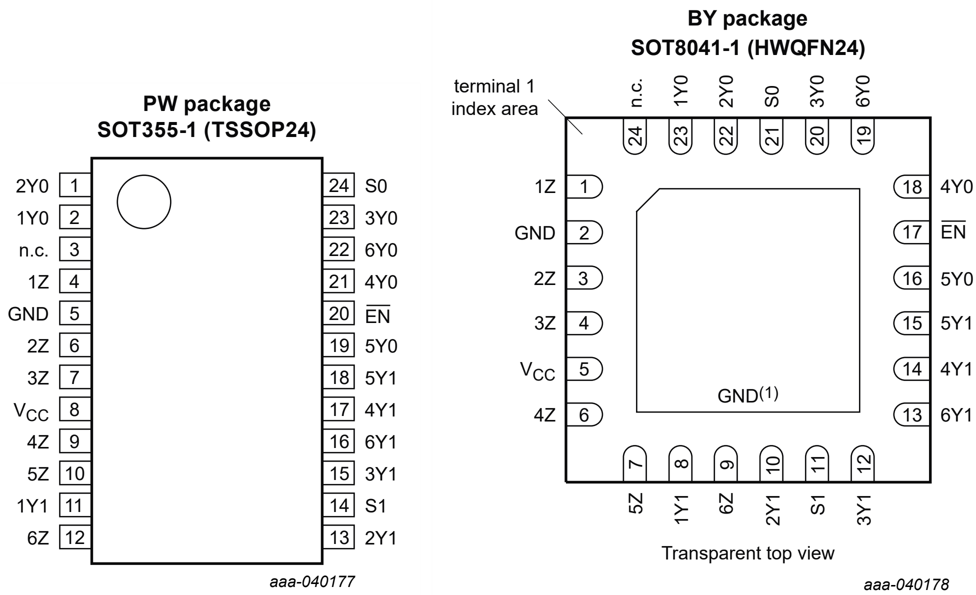


Fig. 1. Logic symbol

7. Pinning information

7.1. Pinning



(1) This is not a supply pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

7.2. Pin description

Table 3. Pin description

Symbol	Pin		Type	Description
	SOT355-1	SOT8041-1		
2Y0	1	22	I/O	Port 2 independent analog channel; normally closed
1Y0	2	23	I/O	Port 1 independent analog channel; normally closed
n.c.	3	24	open	not connected
1Z	4	1	I/O	Port 1 common analog channel
GND	5	2	power	ground (0 V)
2Z	6	3	I/O	Port 2 common analog channel
3Z	7	4	I/O	Port 3 common analog channel
V_{CC}	8	5	power	supply voltage
4Z	9	6	I/O	Port 4 common analog channel
5Z	10	7	I/O	Port 5 common analog channel
1Y1	11	8	I/O	Port 1 independent analog channel; normally open
6Z	12	9	I/O	Port 6 common analog channel
2Y1	13	10	I/O	Port 2 independent analog channel; normally open
S1	14	11	input	select input; do not leave this pin floating
3Y1	15	12	I/O	Port 3 independent analog channel; normally open
6Y1	16	13	I/O	Port 6 independent analog channel; normally open
4Y1	17	14	I/O	Port 4 independent analog channel; normally open

Symbol	Pin		Type	Description
	SOT355-1	SOT8041-1		
5Y1	18	15	I/O	Port 5 independent analog channel; normally open
5Y0	19	16	I/O	Port 5 independent analog channel; normally closed
$\overline{EN}$	20	17	input	enable input (active Low); do not leave this pin floating
4Y0	21	18	I/O	Port 4 independent analog channel; normally closed
6Y0	22	19	I/O	Port 6 independent analog channel; normally closed
3Y0	23	20	I/O	Port 3 independent analog channel; normally closed
S0	24	21	input	select input; do not leave this pin floating

8. Functional description

8.1. Overview

The NMUX27518 is a general purpose, six-channel analog switch with a single pole that can be configured to select between one of two possible connection paths (SPDT). Each analog connection path is bi-directional, with similar electrical characteristics independent of the direction of signal propagation.

8.2. Key features

1.8 V Compatible digital logic thresholds

It is common for modern systems to operate control signals from lower voltage nodes such as 1.8 V, while operating their data signals at higher voltage nodes such as 3.3 V. To remove the requirements for a voltage translation device, the NMUX27518 digital control pins maintain 1.8 V logic compatible thresholds at higher operating voltages, up to 3.63 V. Please note that operating control pins at a lower voltage than the device operating voltage will increase the device supply current, as represented by the datasheet parameter ΔI_{CC}.

I_{off} protection circuitry of digital inputs

The NMUX27518 implements I_{off} protection circuitry on the digital control pins, isolating those pins from the internal circuits when the supply is unpowered (i.e., V_{CC} = 0 V). The ESD protection diodes on the digital input pins do not have a connection path to V_{CC}. If the digital input pins are biased when the V_{CC} pin is unpowered:

1. The high impedance of the digital input pins minimizes input current leakage.
2. The isolation between the digital input pins and the V_{CC} pin ensures no back-powering to the supply rail.

I_{off} protection circuitry of analog inputs/outputs

The NMUX27518 implements I_{off} protection circuitry on the analog switch pins, isolating those pins from the internal circuits when the supply is unpowered (i.e., V_{CC} = 0 V). The ESD protection diodes on the analog switch pins do not have a connection path to V_{CC}. If the analog switch pins are biased when the V_{CC} pin is unpowered:

1. The high impedance of the analog pins minimizes input current leakage.
2. The isolation between the analog pins and the V_{CC} pin ensures no back-powering to the supply rail.
3. The high impedance of the analog switch path itself minimizes signal coupling across the switch.

Support for high speed signals

The NMUX27518 switch bandwidth of 500 MHz reduces the degradation of output rise and fall times, while its 80 ps port skew helps to minimize erosion into the setup and hold time budget.

Function table

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state

Control inputs			Analog channels					
$\overline{EN}$	S0	S1	connection path 1Z	connection path 2Z	connection path 3Z	connection path 4Z	connection path 5Z	connection path 6Z
H	X	X	Hi-Z (all nYn and nZ pins are in high-impedance OFF-state					
L	L	L	1Y0	2Y0	3Y0	4Y0	5Y0	6Y0
L	H	L	1Y1	2Y1	3Y1	4Y0	5Y0	6Y0
L	L	H	1Y0	2Y0	3Y0	4Y1	5Y1	6Y1
L	H	H	1Y1	2Y1	3Y1	4Y1	5Y1	6Y1

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	4.6	V
V_I	input voltage	$\overline{EN}$, S0, S1 [1]	-0.5	4.6	V
V_{SW}	switch voltage	nYn, nZ [2]	-0.5	4.6	V
I_{SW}	switch current	nYn, nZ; V_{SW} > -0.5 V or V_{SW} < V_{CC} + 0.5 V; T_{amb} = -40 °C to +85 °C	-50	50	mA
		nYn, nZ; V_{SW} > -0.5 V or V_{SW} < V_{CC} + 0.5 V; T_{amb} = -40 °C to +125 °C	-25	25	mA
I_I	input current	$\overline{EN}$, S0, S1	-30	30	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [3][4]	-	500	mW

[1] The minimum and maximum input voltage rating may be exceeded if the input clamping current rating is observed.
[2] The minimum and maximum switch voltage rating may be exceeded if the switch clamping current rating is observed.
[3] For SOT355-1 (TSSOP24) package: P_{tot} derates linearly with tbd mW/K above tbd °C.
[4] For SOT8041-1 (HWQFN24) package: P_{tot} derates linearly with tbd mW/K above tbd °C.

10. ESD ratings

Table 6. ESD ratings

Symbol	Parameter	Conditions	Value	Unit
V_{ESD}	electrostatic discharge voltage	HBM: ANSI/ESDA/JEDEC JS-001 class 2	±2000	V
		CDM: ANSI/ESDA/JEDEC JS-002 class C3	±1500	V
		IEC61000-4-2, level 3, contact discharge on all nYn pins	±6000	V

11. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.08	3.63	V
V_I	digital input voltage	$\overline{EN}$, S0, S1	0	3.63	V
V_{SW}	analog switch input voltage	nZ, nYn	0	V_{CC}	V
		V_{CC} = 0 V	0	3.63	V
I_{SW}	analog switch continuous current	nZ, nYn	-50	50	mA
T_{amb}	ambient temperature		-40	+125	°C

12. Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	SOT8041-1 (HWQFN24)	SOT355-1 (TSSOP24)	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.58	81.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.36	36.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.88	2.3	°C/W

13. Static characteristics

Table 9. Static characteristics

At recommended operating conditions; Voltages are referenced to GND (ground 0 V); for test circuit see Fig. 5.
V_{CC} = 1.08 V to 3.63 V, unless otherwise stated.

Symbol	Parameter	Conditions	25 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
Supply Pin								
I_{CC}	supply current	$\overline{EN}$, Sn inputs; V_I = GND or V_{CC}						
		V_{CC} = 3.3 V ± 10%	-	0.005	-	-	1.1	μA
		V_{CC} = 2.5 V ± 10%	-	0.004	-	-	1	μA
		V_{CC} = 1.8 V ± 10%	-	0.003	-	-	0.8	μA
		V_{CC} = 1.2 V ± 10%	-	0.002	-	-	0.7	μA
ΔI_{CC}	supply current increase	$\overline{EN}$, Sn inputs = 1.8 V, V_{CC} = 3.3 V ± 10%	-	4	-	-	9	μA/input
		$\overline{EN}$, Sn inputs = 1.2 V, V_{CC} = 1.8 V ± 10%	-	0.1	-	-	2	μA/input
Control pins								
V_{IH}	HIGH-level input voltage	V_{CC} = 3.3 V ± 10%	-	-	-	1.24	-	V
		V_{CC} = 2.5 V ± 10%	-	-	-	1.07	-	V
		V_{CC} = 1.8 V ± 10%	-	-	-	0.89	-	V
		V_{CC} = 1.2 V ± 10%	-	-	-	0.89	-	V
V_{IL}	LOW level input voltage	V_{CC} = 3.3 V ± 10%	-	-	-	-	0.66	V
		V_{CC} = 2.5 V ± 10%	-	-	-	-	0.56	V
		V_{CC} = 1.8 V ± 10%	-	-	-	-	0.46	V
		V_{CC} = 1.2 V ± 10%	-	-	-	-	0.35	V
I_I	input leakage current	V_I = 0 V, 1.8 V, or V_{CC}	-	-	-	-1	1	μA
C_I	input capacitance	V_I = 0 V or 1.8 V or V_{CC}; f = 1 MHz	-	2	-	-	3	pF
Analog pins								
$R_{ON(peak)}$	ON resistance (peak)	V_I = 0 V to V_{CC}; I_{SW} = 32 mA						
		V_{CC} = 3.3 V ± 10%	-	8	-	-	14	Ω
		V_{CC} = 2.5 V ± 10%	-	11	-	-	20	Ω
		V_{CC} = 1.8 V ± 10%	-	19	-	-	32	Ω
		V_{CC} = 1.2 V ± 10%	-	31	-	-	41	Ω
ΔR_{ON}	ON resistance matching	V_I = 0 V to V_{CC}; I_{SW} = 32 mA						
		V_{CC} = 3.3 V ± 10%	-	0.2	-	-	1.0	Ω
		V_{CC} = 2.5 V ± 10%	-	0.2	-	-	1.0	Ω
		V_{CC} = 1.8 V ± 10%	-	0.6	-	-	3.2	Ω
		V_{CC} = 1.2 V ± 10%	-	0.5	-	-	19	Ω
$R_{ON(flat)}$	ON resistance (flatness)	V_I = 0 V to V_{CC}; I_{SW} = 32 mA						
		V_{CC} = 3.3 V ± 10%	-	2	-	-	5	Ω
		V_{CC} = 2.5 V ± 10%	-	4	-	-	11	Ω
		V_{CC} = 1.8 V ± 10%	-	12	-	-	21	Ω
		V_{CC} = 1.2 V ± 10%	-	21	-	-	27	Ω

Symbol	Parameter	Conditions	25 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
$I_{S(OFF)}$	OFF-state leakage current	nYn OFF						
		V_{CC} = 3.3 V ± 10%; V_I = 1 V; V_O = 2.97 V	-	0.2	-	-500	500	nA
		V_{CC} = 2.5 V ± 10%; V_I = 0.5 V; V_O = 2.25 V	-	0.2	-	-500	500	nA
		V_{CC} = 1.8 V ± 10%; V_I = 0.3 V; V_O = 1.62 V	-	0.2	-	-500	500	nA
		V_{CC} = 1.2 V ± 10%; V_I = 0.1 V; V_O = 1.08 V	-	0.1	-	500	500	nA
$I_{D(OFF)}$	OFF-state leakage current	nZ OFF						
		V_{CC} = 3.3 V ± 10%; V_I = 1 V; V_O = 2.97 V	-	0.2	-	-500	500	nA
		V_{CC} = 2.5 V ± 10%; V_I = 0.5 V; V_O = 2.25 V	-	0.2	-	-500	500	nA
		V_{CC} = 1.8 V ± 10%; V_I = 0.3 V; V_O = 1.62 V	-	0.2	-	-500	500	nA
		V_{CC} = 1.2 V ± 10%; V_I = 0.1 V; V_O = 1.08 V	-	0.1	-	500	500	nA
$I_{S(ON)}$	ON-state leakage current	nYn ON						
		V_{CC} = 3.3 V ± 10%; V_I = 1 V or 2.97 V; V_O = open	-	0.2	-	-500	500	nA
		V_{CC} = 2.5 V ± 10%; V_I = 0.5 V or 2.25 V; V_O = open	-	0.2	-	-500	500	nA
		V_{CC} = 1.8 V ± 10%; V_I = 0.3 V or 1.62 V; V_O = open	-	0.2	-	-500	500	nA
		V_{CC} = 1.2 V ± 10%; V_I = 0.1 V or 1.08 V; V_O = open	-	0.1	-	500	500	nA
$I_{D(ON)}$	ON-state leakage current	nZ ON						
		V_{CC} = 3.3 V ± 10%; V_I = 1 V or 2.97 V; V_O = open	-	0.2	-	-500	500	nA
		V_{CC} = 2.5 V ± 10%; V_I = 0.5 V or 2.25 V; V_O = open	-	0.2	-	-500	500	nA
		V_{CC} = 1.8 V ± 10%; V_I = 0.3 V or 1.62 V; V_O = open	-	0.2	-	-500	500	nA
		V_{CC} = 1.2 V ± 10%; V_I = 0.1 V or 1.08 V; V_O = open	-	0.1	-	500	500	nA
$I_{S(POFF)}$	power-OFF leakage current	nYn; V_{CC} = 0 V						
		V_I = 0 V to 3.63 V; V_O = 0 V	-	2.6	-	-1	6	μA
		V_I = 0 V to 3.63 V; V_O = 3.63 V to 0 V	-	2.6	-	-1	6	μA
		V_I = 0 V to 2.75 V; V_O = 0 V	-	1.4	-	-1	3	μA
		V_I = 0 V to 2.75 V; V_O = 2.75 V to 0 V	-	1.4	-	-1	3	μA
		V_I = 0 V to 1.98 V; V_O = 0 V	-	0.6	-	-1	1	μA
		V_I = 0 V to 1.98 V; V_O = 1.98 V to 0 V	-	0.6	-	-1	1	μA
		V_I = 0 V to 1.32 V; V_O = 0 V	-	0.1	-	-1	1	μA
		V_I = 0 V to 1.32 V; V_O = 1.32 V to 0 V	-	0.1	-	-1	1	μA

Symbol	Parameter	Conditions	25 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
$I_{D(POFF)}$	power-OFF leakage current	nZ; V_{CC} = 0 V						
		V_I = 0 V to 3.63 V; V_O = 0 V	-	2.6	-	-1	11	μA
		V_I = 0 V to 3.63 V; V_O = 3.63 V to 0 V	-	2.6	-	-1	11	μA
		V_I = 0 V to 2.75 V; V_O = 0 V	-	1.4	-	-1	6	μA
		V_I = 0 V to 2.75 V; V_O = 2.75 V to 0 V	-	1.4	-	-1	6	μA
		V_I = 0 V to 1.98 V; V_O = 0 V	-	0.6	-	-1	6	μA
		V_I = 0 V to 1.98 V; V_O = 1.98 V to 0 V	-	0.5	-	-1	2	μA
		V_I = 0 V to 1.32 V; V_O = 0 V	-	0.1	-	-1	6	μA
		V_I = 0 V to 1.32 V; V_O = 1.32 V to 0 V	-	0.1	-	-1	1	μA

14. Dynamic characteristics

Table 10. Dynamic characteristics

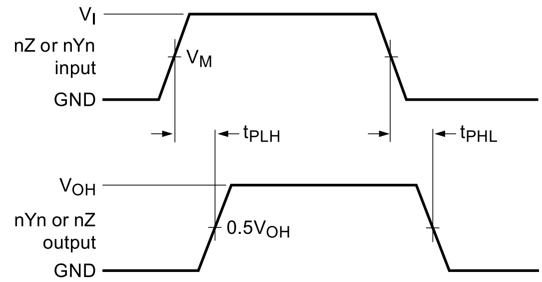
At recommended operating conditions; voltages are referenced to GND (ground 0 V); V_{CC} = 1.08 V to 3.63 V, unless otherwise stated; for test circuit see Fig. 5.

Symbol	Parameter	Conditions	25 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
Analog pins								
t_t	transition time between channels	Sn to nZ channel; nY0 = 0 V and nY1 = V_{CC}; nY0 = V_{CC} and nY1 = 0 V; R_L = 50 Ω; C_L = 35 pF						
		V_{CC} = 3.3 V ± 10%	-	15	-	-	22	ns
		V_{CC} = 2.5 V ± 10%	-	18	-	-	26	ns
		V_{CC} = 1.8 V ± 10%	-	20	-	-	35	ns
		V_{CC} = 1.2 V ± 10%	-	37	-	-	75	ns
		Sn to nYn channel; nZ = V_{CC}; R_L = 50 Ω; C_L = 35 pF						
		V_{CC} = 3.3 V ± 10%	-	16	-	-	22	ns
		V_{CC} = 2.5 V ± 10%	-	18	-	-	26	ns
		V_{CC} = 1.8 V ± 10%	-	22	-	-	35	ns
		V_{CC} = 1.2 V ± 10%	-	43	-	-	75	ns
t_{b-m}	break before make time	nZ; V_I = V_{CC}; R_L = 50 Ω; C_L = 35 pF						
		V_{CC} = 3.3 V ± 10%	-	10	-	1	-	ns
		V_{CC} = 2.5 V ± 10%	-	11	-	1	-	ns
		V_{CC} = 1.8 V ± 10%	-	12	-	1	-	ns
		V_{CC} = 1.2 V ± 10%	-	19	-	1	-	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
t_{en}	enable time	$\overline{EN}$ to nZ or nYn; $V_I = V_{CC}$; $R_L = 50\ \Omega$; $C_L = 35$ pF; S1 = GND						
		$V_{CC} = 3.3$ V ± 10%	-	6	-	-	11	ns
		$V_{CC} = 2.5$ V ± 10%	-	8	-	-	14	ns
		$V_{CC} = 1.8$ V ± 10%	-	13	-	-	24	ns
		$V_{CC} = 1.2$ V ± 10%	-	32	-	-	78	ns
		$\overline{EN}$ to nZ or nYn; $V_I = V_{CC}$; $R_L = 50\ \Omega$; $C_L = 35$ pF; S1 = V_{CC}						
		$V_{CC} = 3.3$ V ± 10%	-	6	-	-	10	ns
		$V_{CC} = 2.5$ V ± 10%	-	8	-	-	14	ns
		$V_{CC} = 1.8$ V ± 10%	-	11	-	-	23	ns
		$V_{CC} = 1.2$ V ± 10%	-	26	-	-	72	ns
t_{dis}	disable time	$\overline{EN}$ to nZ or nYn; $V_I = V_{CC}$; $R_L = 50\ \Omega$; $C_L = 35$ pF; S1 = GND						
		$V_{CC} = 3.3$ V ± 10%	-	4	-	-	7	ns
		$V_{CC} = 2.5$ V ± 10%	-	5	-	-	8	ns
		$V_{CC} = 1.8$ V ± 10%	-	7	-	-	12	ns
		$V_{CC} = 1.2$ V ± 10%	-	32	-	-	69	ns
		$\overline{EN}$ to nZ or nYn; $V_I = V_{CC}$; $R_L = 50\ \Omega$; $C_L = 35$ pF; S1 = V_{CC}						
		$V_{CC} = 3.3$ V ± 10%	-	9	-	-	11	ns
		$V_{CC} = 2.5$ V ± 10%	-	10	-	-	14	ns
		$V_{CC} = 1.8$ V ± 10%	-	12	-	-	22	ns
		$V_{CC} = 1.2$ V ± 10%	-	19	-	-	51	ns
$t_{SK(P)}$	port skew	between nZ pins; between nY0 pins; between nY1 pins; $V_I = 0$ V to V_{CC}, 1 MHz digital clock, 1 ns rise/ fall time						
		$V_{CC} = 3.3$ V ± 10%	-	150	-	-	500	ps
		$V_{CC} = 2.5$ V ± 10%	-	130	-	-	500	ps
		$V_{CC} = 1.8$ V ± 10%	-	110	-	-	500	ps
Q_{inj}	charge injection	$V_{gen} = 0$ V; $R_{gen} = 0\ \Omega$; $C_L = 0.1$ nF						
		$V_{CC} = 3.3$ V	-	0.2	-	-	-	pC
		$V_{CC} = 2.5$ V	-	0.1	-	-	-	pC
		$V_{CC} = 1.8$ V	-	0.1	-	-	-	pC
		$V_{CC} = 1.2$ V	-	0.2	-	-	-	pC
α_{iso}	isolation (OFF-state)	$R_L = 50\ \Omega$; $C_L = 5$ pF; f = 10 MHz; $V_{I(DC)} = 0.5 \times V_{CC}$; $V_{I(AC)} = 200$ mV(p-p)						
		$V_{CC} = 3.3$ V	-	-59	-	-	-	dB
		$V_{CC} = 2.5$ V	-	-57	-	-	-	dB
		$V_{CC} = 1.8$ V	-	-54	-	-	-	dB
		$V_{CC} = 1.2$ V	-	-50	-	-	-	dB

Symbol	Parameter	Conditions	25 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
Xtalk	crosstalk	between any two analog pins; R_L = 50 Ω; C_L = 5 pF; f = 10 MHz; $V_{I(DC)}$ = 0.5 × V_{CC}; $V_{I(AC)}$ = 200 mV(p-p)						
		V_{CC} = 3.3 V	-	-58	-	-	-	dB
		V_{CC} = 2.5 V	-	-58	-	-	-	dB
		V_{CC} = 1.8 V	-	-58	-	-	-	dB
		V_{CC} = 1.2 V	-	-58	-	-	-	dB
		between adjacent analog pins; R_L = 50 Ω; C_L = 5 pF; f = 10 MHz; $V_{I(DC)}$ = 0.5 × V_{CC}; $V_{I(AC)}$ = 200 mV(p-p)						
		V_{CC} = 3.3 V	-	-65	-	-	-	dB
		V_{CC} = 2.5 V	-	-65	-	-	-	dB
		V_{CC} = 1.8 V	-	-65	-	-	-	dB
		V_{CC} = 1.2 V	-	-65	-	-	-	dB
BW	bandwidth	R_L = 50 Ω; C_L = 5 pF; $V_{I(DC)}$ = 0.5xV_{CC}; $V_{I(AC)}$ = 200 mV(p-p)						
		V_{CC} = 3.3 V	-	500	-	-	-	MHz
		V_{CC} = 2.5 V	-	500	-	-	-	MHz
		V_{CC} = 1.8 V	-	500	-	-	-	MHz
		V_{CC} = 1.2 V	-	500	-	-	-	MHz
$C_{S(OFF)}$	OFF-state capacitance	nYn OFF; V_I = 0.5 × V_{CC}; f = 1 MHz						
		V_{CC} = 3.3 V	-	8	-	-	-	pF
		V_{CC} = 2.5 V	-	8	-	-	-	pF
		V_{CC} = 1.8 V	-	8	-	-	-	pF
		V_{CC} = 1.2 V	-	8	-	-	-	pF
$C_{D(OFF)}$	OFF-state capacitance	nZ OFF; V_I = 0.5 × V_{CC}; f = 1 MHz						
		V_{CC} = 3.3 V	-	13	-	-	-	pF
		V_{CC} = 2.5 V	-	13	-	-	-	pF
		V_{CC} = 1.8 V	-	14	-	-	-	pF
		V_{CC} = 1.2 V	-	15	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance	nYn ON; V_I = 0.5 × V_{CC}; f = 1 MHz						
		V_{CC} = 3.3 V	-	22	-	-	-	pF
		V_{CC} = 2.5 V	-	22	-	-	-	pF
		V_{CC} = 1.8 V	-	23	-	-	-	pF
		V_{CC} = 1.2 V	-	24	-	-	-	pF
$C_{D(ON)}$	ON-state capacitance	nZ ON; V_I = 0.5 × V_{CC}; f = 1 MHz						
		V_{CC} = 3.3 V	-	22	-	-	-	pF
		V_{CC} = 2.5 V	-	22	-	-	-	pF
		V_{CC} = 1.8 V	-	23	-	-	-	pF
		V_{CC} = 1.2 V	-	24	-	-	-	pF
THD	total harmonic distortion	R_L = 600 Ω; C_L = 50 pF; f = 20 Hz - 20 kHz						
		V_{CC} = 3.3 V	-	0.46	-	-	-	%
		V_{CC} = 2.5 V	-	0.29	-	-	-	%
		V_{CC} = 1.8 V	-	0.28	-	-	-	%
		V_{CC} = 1.2 V	-	0.98	-	-	-	%

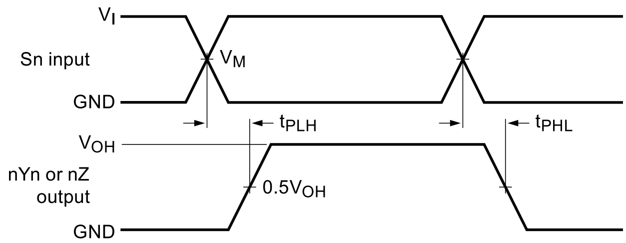
14.1. Waveforms and test circuit



Measurement points are given in Table 11.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

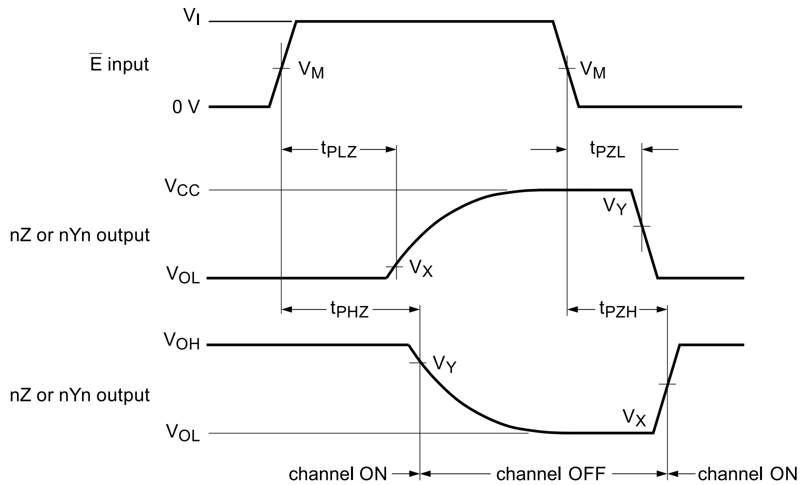
Fig. 2. Input (nZ, nYn) to output (nYn, nZ) propagation delays



Measurement points are given in Table 11.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 3. Input (Sn) to output (nYn, nZ) propagation delays



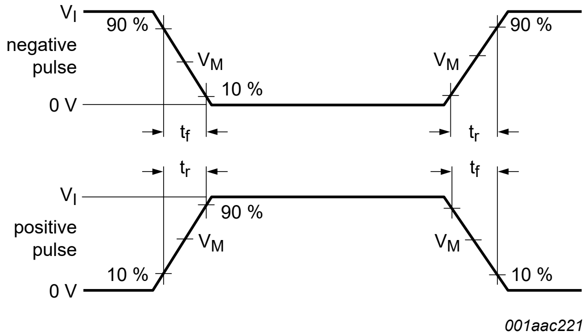
Measurement points are given in Table 11.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

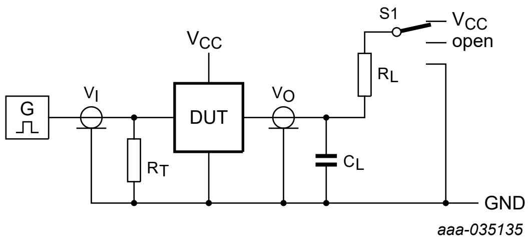
Fig. 4. Enable and disable times

Table 11. Measurement points

Input		Output	
V_M	V_I	V_X	V_Y
0.5 × V_{CC}	V_{CC}	V_{OL} + 0.1(V_{CC} - V_{OL})	0.9 × V_{OH}



a. Input pulse definition



b. Test circuit

Test data is given in Table 12.

Definitions for test circuit:

R_L = load resistance;

C_L = load capacitance including jig and probe capacitance;

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

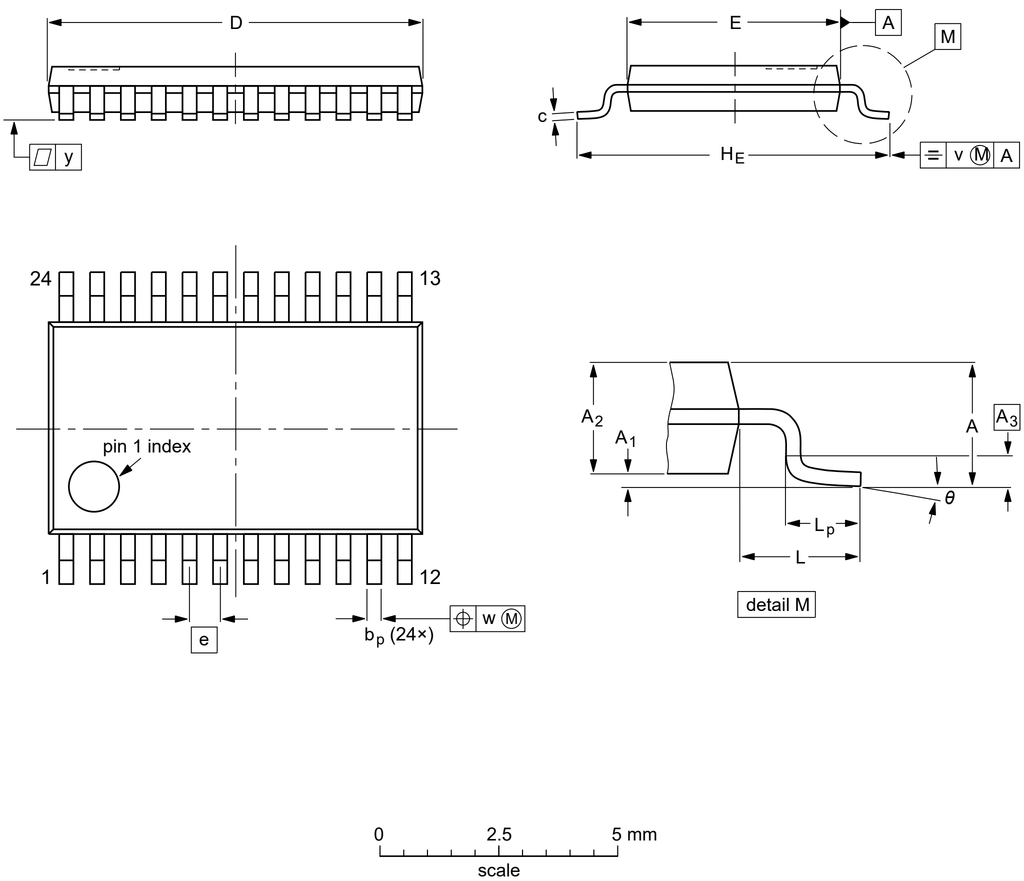
Fig. 5. Test circuit for measuring switching times

Table 12. Test data

Test	Input			Output		S1 position
	Control $\overline{E}$, Sn	Switch nYn (nZ)	t_r, t_f	Switch nZ (nYn)		
	V_I	V_I		C_L	R_L	
t_{PHL}, t_{PLH}	V_{CC}	V_{CC}	< 5 ns	50 pF	-	open
t_{PHZ}, t_{PZH}	V_{CC}	V_{CC}	< 5 ns	50 pF	10 kΩ	GND
t_{PLZ}, t_{PZL}	V_{CC}	V_{CC}	< 5 ns	50 pF	10 kΩ	V_{CC}

15. Package outline

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.20	7.90	4.50		6.60		0.75				8°
	nom				0.25 BSC					0.65 BSC		1.00 REF		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	7.70	4.30		6.20		0.45				0°

Notes

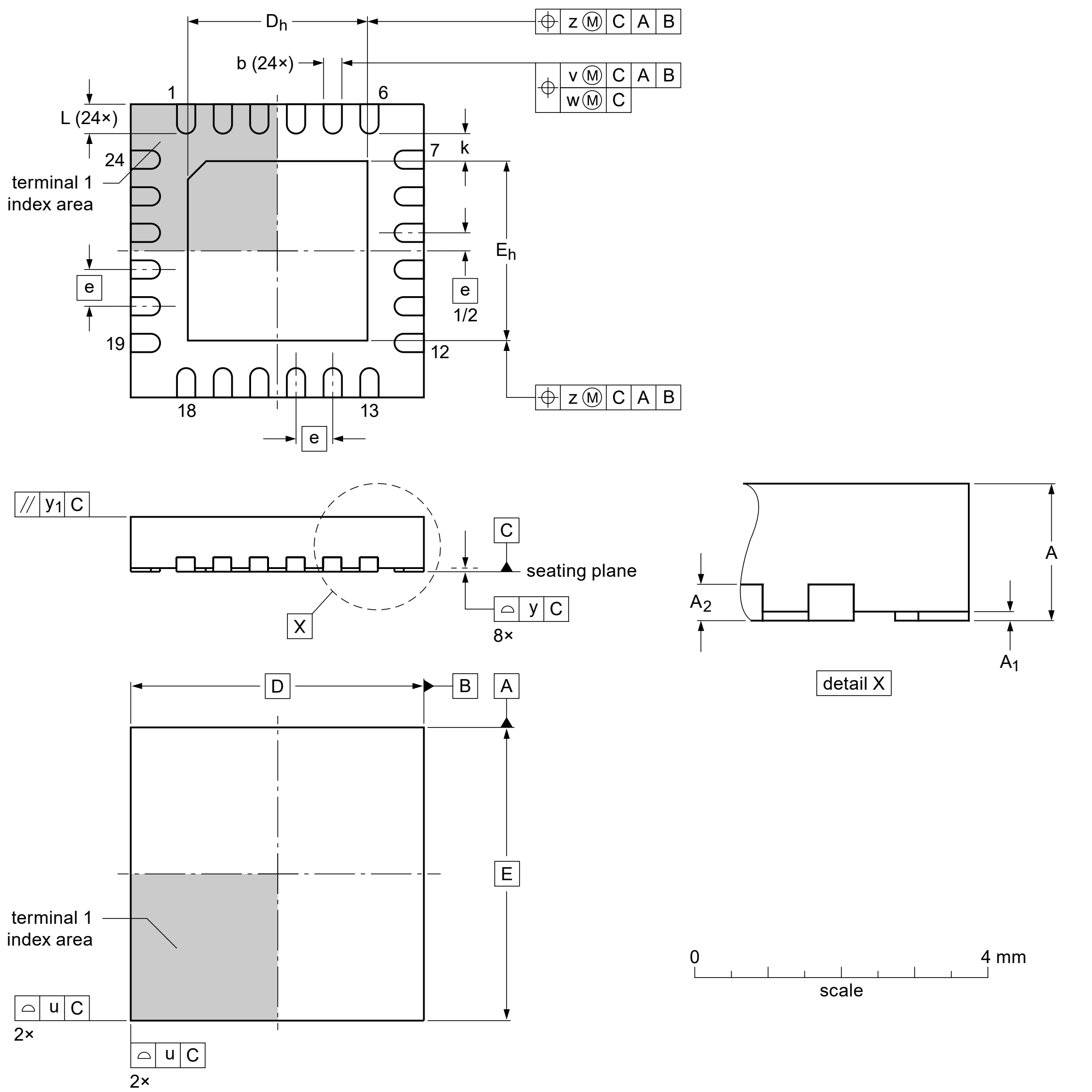
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot355-1_po

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153				~~03-02-19~~ 24-11-07

Fig. 6. Package outline SOT355-1 (TSSOP24)

HWQFN24: plastic thermal enhanced very very thin Quad Flat packages, no leads; 24 terminals; 0.5 mm pitch; 4 x 4 x 0.75 mm body **SOT8041-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	D_h	E	E_h	e	k	L	u	v	w	y	y_1	z
mm	max	0.80	0.05	0.2 Ref.	0.30	4 BSC	2.55	4 BSC	2.55	0.5 BSC	0.375 Ref.	0.50	0.10	0.10	0.05	0.08	0.10	0.10
	nom	0.75			0.25		2.45		2.45			0.40						
	min	0.70	0.00		0.20		2.35		2.35			0.30						

sot8041-1_po

Outline version	References: IEC	References: JEDEC	References: JEITA		European projection	Issue date
SOT8041-1		MO-220 (WGGD-8)				~~22-04-01~~ 22-04-25

Fig. 7. Package outline SOT8041-1 (HWQFN24)

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16. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
qSPI	Quad Serial Peripheral Interface

17. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NMUX27518 v. 1	20250725	Product data sheet	-	-

18. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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